Q.P. Code: 18EC0443 **R18**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Regular Examinations Nov/Dec 2019

ANALOG ELECTRONIC CIRCUITS

(EEE, CSE & CSIT)

Time: 3 hours Max. Marks: 60

PART-A

(Answer all the Questions **5 x 2 = 10** Marks)

1	**a**	Define and draw the series diode clipper.	**2M**
	b	Write the relationship between α, β, ɤ.	**2M**
	c	compare JFET with MOSFET.	**2M**
	d	Define PSRR and Thermal drift.	**2M**
	e	Find the resolution of a 12-bit DAC converter.	**2M**

PART-B

(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2	**a**	Calculate the ripple factor of a LC filter with FWR for a inductance of 10H and capacitance of 8μF for 50Hz AC input supply. Draw the neat circuit diagram.	**5M**
	b	Explain diode positive shunt clippers with waveforms.	**5M**

OR

3	**a**	Explain the working of capacitor filter with circuit diagram.	**5M**
	b	What is clamping circuit? Explain the negative clamping circuits with necessary waveforms.	**5M**

UNIT-II

4	**a**	Define Transistor Biasing and explain the need for Biasing?	**4M**
	b	With neat diagram, explain the Input and Output characteristics of a BJT in CB Configuration.	**6M**

OR

5	**a**	Mention different types of Biasing a Transistor and explain the voltage divider Bias of a Transistor.	**5M**
	b	Explain the concept of Load line and Q-point in BJT.	**5M**

UNIT-III

6	**a**	Discuss JFET Fixed Bias with neat diagram and derive the expression for Input impedance, Output impedance and Voltage gain.	**6M**
	b	Draw and explain the small signal model of FET at low frequency.	**4M**

OR

7	**a**	Discuss the operation and characteristics of n-channel depletion type MOSFET with diagram.	**7M**
	b	Mention the applications of JFET.	**3M**

UNIT-IV

8	**a**	What is frequency compensation and explain how the frequency response is varied with respect to Compensation network	**6M**
	b	An op-amp has a slew rate of 2V/μs. What is the maximum frequency of an output sinusoid of peak value 5V at which the distortion sets in due to the slew rate limitation.	**4M**

OR

9	**a**	Explain ac characteristics of op-amp.	**5M**
	b	Explain the necessity of level translator stage in cascading differential amplifiers.	**5M**

UNIT-V

10	**a**	Draw a neat circuit of a differentiator circuit. Explain the functioning with the input-output Waveforms.	**5M**
	b	What is regulator and explain IC 723.	**5M**
		OR	
11	**a**	Design a first order high pass filter for a cutoff frequency of 100 Hz and gain 2 draw the circuit diagram.	**5M**
	b	Draw and explain the weighted resistor DAC.	**5M**

END